

What is claimed is:

- 1 1. A method of forming a transistor, comprising:
- 2 forming a silicidation barrier on a patterned polysilicon layer;
- 3 implanting dopants to form a source/drain extension layer self-aligned to
- 4 the patterned polysilicon;
- 5 forming a first silicide layer over the source/drain extension layer;
- 6 forming sidewall spacers adjacent to the patterned polysilicon;
- 7 removing a portion of the silicidation barrier from a top surface of the
- 8 patterned polysilicon;
- 9 forming a second silicide layer self-aligned to the sidewall spacers; and
- 10 forming a third silicide layer on a top surface of the patterned polysilicon.
- 1 2. The method of Claim 1 wherein the second silicide layer and the third
- 2 silicide layer are formed concurrently.
- 1 3. The method of Claim 1, wherein forming a silicidation barrier comprises
- 2 nitridizing the patterned polysilicon layer.
- 1 4. The method of Claim 1, wherein forming the silicidation barrier comprises
- 2 forming a silicon nitride layer on a top surface of the patterned polysilicon, and
- 3 on at least one sidewall of the patterned polysilicon.

- 1 5. The method of Claim 1, wherein the silicidation barrier has a thickness  
2 sufficient to prevent silicidation of the polysilicon.
- 1 6. The method of Claim 1, further comprising depositing a layer of metal over  
2 the source/drain extension layer, wherein the metal is selected from the group  
3 consisting of titanium and cobalt.
- 1 7. The method of Claim 6, wherein further comprising depositing a layer of  
2 metal over the first silicide layer, wherein the metal is selected from the group  
3 consisting of nickel and cobalt.
- 1 8. The method of Claim 1, wherein the second and third silicide layers  
2 comprise nickel silicide.
- 1 9. The method of Claim 1, further comprising implanting dopants through the  
2 first silicide layer to form source/drains self-aligned to the sidewall spacers.
- 1 10. A method of forming a microelectronic device, comprising:  
2 forming a patterned polysilicon layer over a dielectric layer, the dielectric  
3 layer disposed on a substrate, the patterned polysilicon having sidewalls and a  
4 top surface;  
5 nitridizing the sidewalls and top surface of the polysilicon;

6        implanting first dopants into the substrate to form a source/drain extension  
7 layer;  
8        forming a first silicide layer over the source/drain extension layer;  
9        forming sidewall spacers adjacent to the sidewalls;  
10       implanting second dopants through the first silicide layer into a  
11 source/drain region; and  
12       forming a second silicide self-aligned to the sidewall spacers.

1    11.    The method of Claim 10, further comprising thermally activating the first  
2 dopants prior to implanting the second dopant atoms.

1    12.    The method of Claim 10 wherein the first and second silicides comprise  
2 different metals.

1    13.    The method of Claim 10 wherein the first and second silicides comprise  
2 the same metal.

1    14.    The method of Claim 10 wherein nitridizing the polysilicon produces a  
2 silicon nitride layer approximately 10 angstroms thick.

1    15.    The method of Claim 10, further comprising forming an agglomeration-  
2 free silicide layer over the patterned polysilicon.

1 16. The method of Claim 10, further comprising removing the nitridized  
2 portion of the top surface of the gate electrode.

1 17. The method of Claim 10, wherein the second silicide layer is formed  
2 through the first silicide layer.

1 18. A microelectronic structure, comprising:  
2 a gate electrode having sidewalls;  
3 a silicidation barrier adjacent to the sidewalls;  
4 a first silicide layer superjacent the gate electrode; and  
5 a pair of source/drain terminals self-aligned to the gate electrode;  
6 wherein the source/drain terminals comprise a first implanted region, a second  
7 silicide layer; a second implanted regions and a third silicide layer.

1 19. The microelectronic structure of Claim 18, wherein the second silicide  
2 layer is contained within the first implanted region.

1 20. The microelectronic structure of Claim 18, wherein the third silicide layer is  
2 thicker than the first implanted region.

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B1

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D3  
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E1